LME49990

LME49990 Overture E-Series Ultra-low Distortion, Ultra-low Noise

Operational Amplifier

TEXAS INSTRUMENTS

Literature Number: SNOSB16B

Ultra-low Distortion, Ultra-low Noise Operational Amplifier

General Description

The LME49990 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. The LME49990 combines low voltage noise density ($0.9nV/\sqrt{Hz}$) with vanishing low THD+N (0.00001%). The LME49990 has a high slew rate of $\pm22V/\mu s$ and an output current capability of $\pm27mA$. It drives 600Ω loads to within 2V of either power supply voltage.

The LME49990's outstanding Gain (135dB), CMRR (137dB), PSRR (144dB), and V_{OS} (130μV) give the amplifier excellent operational amplifier DC performance. The LME49990 has a wide supply range of $\pm5V$ to $\pm18V$. The LME49990 is unity gain stable and is available in an 8-lead narrow body SOIC and LLP.

Key Specifications

- Input Noise Density (f = 1kHz) $0.9nV/\sqrt{Hz}$ (typ)
  $1.3nV/\sqrt{Hz}$ (max)

- THD+N
  ($A_V = 1$, $V_{OUT} = 3V_{RMS}$, $f_{IN} = 1kHz$)
  $R_L = 600\Omega$ 0.00001%

- 1/f Corner Frequency 43Hz (typ)

- Slew Rate $\pm22V/\mu s$ (max)

- Gain Bandwidth
  ($A_V = 10^4$, $R_L = 2k\Omega$, f = 90kHz) 110MHz (typ)

- PSRR 144dB (typ)

- CMRR 137dB (typ)

- Power Supply Voltage Range $\pm5V$ to $\pm18V$

Features

- Easily drives 600Ω load
- Output short circuit protection

Applications

- Ultra high quality audio signal processing
- Active Filters
- Preamplifiers
- Spectrum analyzers
- Ultrasound preamplifiers
- Sigma-Delta ADC/DAC buffers
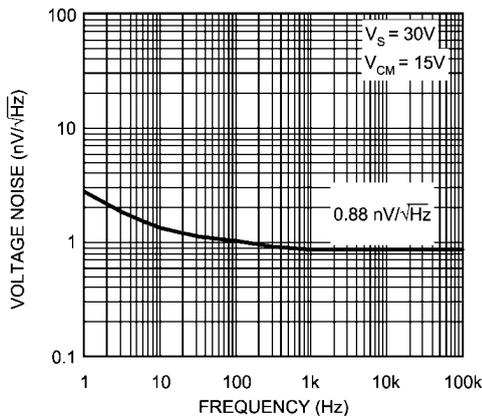- The exposed pad (DAP) of unit should NOT be grounded. It is internally connected to V_{EE}.
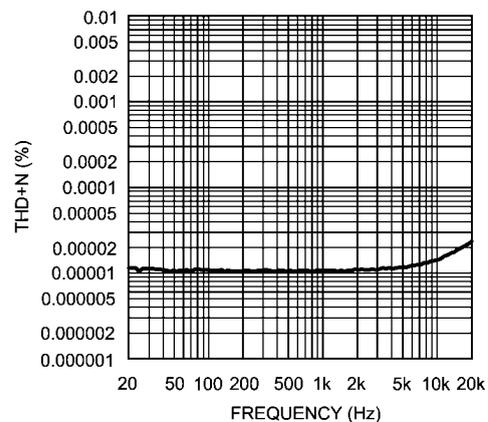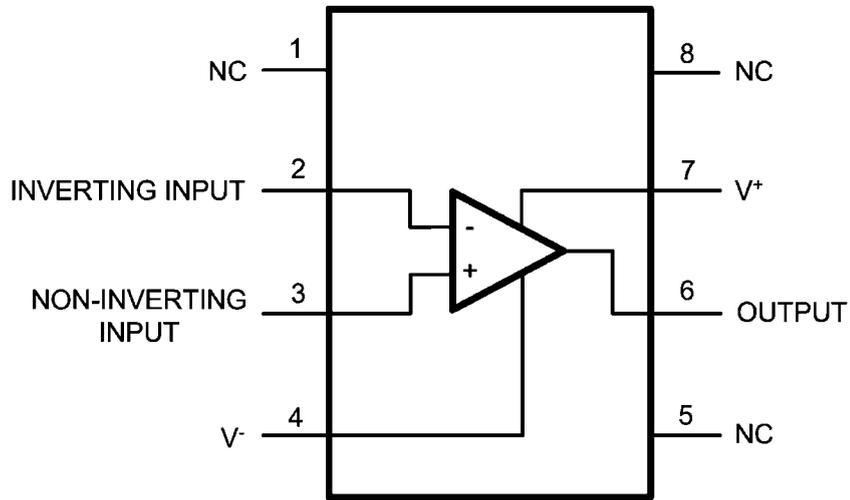

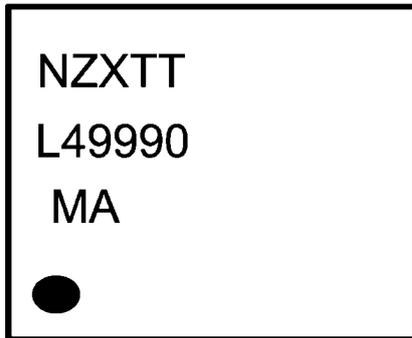FIGURE 1: Voltage Noise Spectral Density

FIGURE 2. THD+N vs Frequency

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Connection Diagrams

Order Number LME49990MA
See NS Package Number — M08A
Order Number LME49990SD
See NS Package Number — SDB08B

30059702

LME49990MA (SOIC) Top Mark

NZXTT

L49990

MA

300597g0

N = National logo
Z = Assembly plant code
X = 1 Digit date code
TT = Die traceability
L49990 = LME49990
MA = Package code

LME49990SD (LLP) Top Mark

N

ZXTT

49990

300597g1

N = National logo
Z = Assembly plant code
X = 1 Digit date code
TT = Die traceability
49990 = LME49990

Ordering Information

Order Number	Package	Package DWG #	Transport Media	MSL Level
LME49990MA	8L SOIC	M08A	95 units in reel	1
LME49990MAX	8L SOIC	M08A	2500 units in tape and reel	1
LME49990SDE	8L LLP	SDB08B	250 units in tape and reel	1
LME49990SD	8L LLP	SDB08B	1000 units in tape and reel	1
LME49990SDX	8L LLP	SDB08B	4500 units in tape and reel	1

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage
($V_S = V^+ - V^-$)   38V
Storage Temperature   −65°C to 150°C
Input Voltage   (V-) - 0.3V to (V+) + 0.3V
Output Short Circuit (*Note 3*)   Continuous
Power Dissipation   Internally Limited
ESD Rating (*Note 4*)   2000V
ESD Rating (*Note 5*)   200V
ESD Rating (*Note 8*)   1000V

Junction Temperature   150°C
Thermal Resistance
  θ_{JA} (SO)   145°C/W
  θ_{JA} (LLP)   52.5°C/W
Soldering Information
  Infrared or Convection (20 sec)   260°C

Operating Ratings (*Note 1*)

Temperature Range
  $T_{MIN} \leq T_A \leq T_{MAX}$ −40°C ≤ T_A ≤ 85°C
Supply Voltage Range   ±5V ≤ V_S ≤ ±18V

Electrical Characteristics (*Note 2*)

The following specifications apply for $V_S = \pm15V$, $R_L = 2k\Omega$, $f_{IN} = 1kHz$, and $T_A = 25°C$, unless otherwise specified.

Symbol	Parameter	Conditions	LME49990 Typical (*Note 6*)	LME49990 Limit (*Note 7*)	Units (Limits)
POWER SUPPLY					
V_{CC}	Operating Supply Voltage			±5 ±18	V (min) V (max)
I_{CCQ}	Quiescent Current	$V_{CM} = 0V$, $V_O = 0V$, $I_O = 0mA$ $V_{CC} = \pm5V$ $V_{CC} = \pm15V$ $V_{CC} = \pm18V$	 8 9 9	 10 11 12	 mA (max)
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm5V$ to $\pm18V$ $T_{MIN}-T_{MAX}$	144 137	119 116	dB (min) dB (min)
DYNAMIC PERFORMANCE					
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$, $V_O = 3V_{RMS}$, $R_L = 1k\Omega$ f = 1kHz f = 20kHz	 0.00001 0.00003	 0.00002 	 % (max) %
IMD	Intermodulation Distortion	$A_V = 1$, $V_O = 3V_{RMS}$ Two-tone 60Hz & 7kHz 4:1	 0.000017		 %
GBWP	Gain Bandwith Product	$A_V = 10^4$, $R_L = 2k\Omega$, f = 90kHz	110		MHz
FPBW	Full Power Bandwidth	$A_V = -1$, $V_O = 20V_{PP}$, $R_L = 1k\Omega$	291		kHz
SR	Slew Rate	$A_V = -1$, $V_O = 20V_{PP}$ $R_L = 1k\Omega$	 22	 16.5	V/µs (min)
t_s	Settling time	$A_V = -1$, $V_O = 10V_{PP}$, $R_L = 1k\Omega$ 0.01%	 590		 ns
A_{VOL}	Open-Loop Gain	$V_O = \pm10V$ $R_L = 2k\Omega$ $T_{MIN} - T_{MAX}$ $R_L = 600\Omega$ $T_{MIN} - T_{MAX}$	 135 124 130 122	 120 120 	 dB (min) dB dB (min) dB

Symbol	Parameter	Conditions	LME49990 Typical (Note 6)	Limit (Note 7)	Units (Limits)
NOISE					
e_N	Input Noise Voltage Density	f = 10Hz	1.4		nV/$\sqrt{\text{Hz}}$
		f = 100Hz	1.0		nV/$\sqrt{\text{Hz}}$
		f = 1kHz	0.88	1.3	nV/$\sqrt{\text{Hz}}$ (max)
		f = 10kHz	0.88		nV/$\sqrt{\text{Hz}}$
V_NOISE	RMS Voltage Noise	BW = 0.1Hz to 10Hz	30		nV$_{PP}$
		BW = 10Hz to 20kHz	0.12	0.2	μV (max)
		BW = 10Hz to 1MHz	1	1.2	μV (max)
i_N	Input Current Noise Density	f = 1kHz	2.8		pA/$\sqrt{\text{Hz}}$
INPUT CHARACTERISTICS					
V_{OS}	Offset Voltage	V_{CC} = ±18V, V_{CM} = 0v, V_O = 0V	130	1000	μV (max)
		V_{CC} = ±18V, $T_{MIN} - T_{MAX}$	300	2000	μV (max)
V_{OS} Drift	Input Offset Voltage Drift vs Temperature ($\Delta V_{OS}/\Delta$Temp)	V_{CC} = ±18V, $T_{MIN} - T_{MAX}$	2		μV/°C
I_{BIAS}	Input Bias Current	V_{CC} = ±18V, V_{CM} = 0v, V_O = 0V	30	500	nA (max)
		V_{CC} = ±18V, $T_{MIN} - T_{MAX}$	150	1000	nA (max)
I_{OS}	Input Offset Current	V_{CC} = ±18V, V_{CM} = 0v, V_O = 0V	35	400	nA (max)
		V_{CC} = ±18V, $T_{MIN} - T_{MAX}$	95	1000	nA (max)
V_{IN-CM}	Common-Mode Input Voltage Range		12	11	V (min)
CMRR	Common-Mode Rejection	−10V<V_{CM}<10V	137	118	dB (min)
		$T_{MIN} - T_{MAX}$	132	110	dB (min)
OUTPUT CHARACTERISTICS					
V_{OUT}	Output Voltage Swing	V_{CC} = ±15V, R_L = 2kΩ	±13	12.5	V (min)
		V_{CC} = ±15V, R_L = 600Ω	±13	12	V (min)
		V_{CC} = ±18V, R_L = 600Ω	±16	14.0	V (min)
I_{SHIRT}	Output Short-Circuit Current	V_{CC} = ±18V	+75/-70	+55/-50	mA (min)
I_{OUT}	Output Current	V_{CC} = ±18V, R_L = 600Ω	26	24	mA (min)

Note 1: "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Amplifier output connected to GND, any number of amplifiers within a package.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Note 8: Charge device model, applicable std JESD22–C101–A.

Typical Performance Characteristics

THD+N vs Output Voltage
$V_{CC} = -V_{EE} = 15V$, $R_L = 2k\Omega$

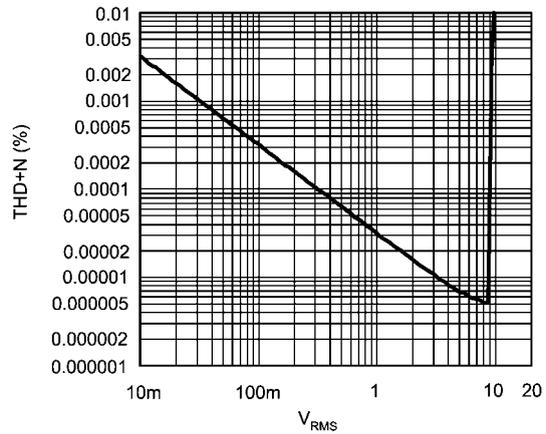**THD+N vs Output Voltage**
$V_{CC} = -V_{EE} = 18V$, $R_L = 2k\Omega$

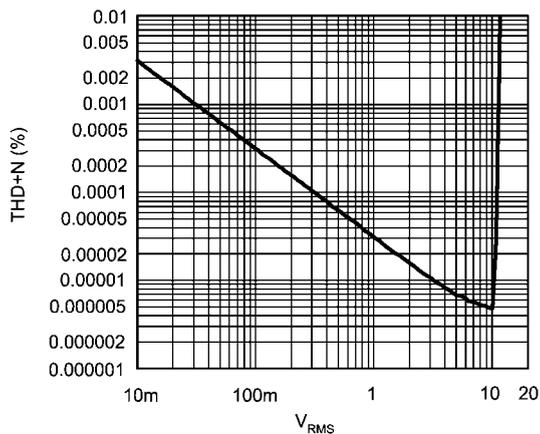**THD+N vs Output Voltage**
$V_{CC} = -V_{EE} = 5V$, $R_L = 2k\Omega$

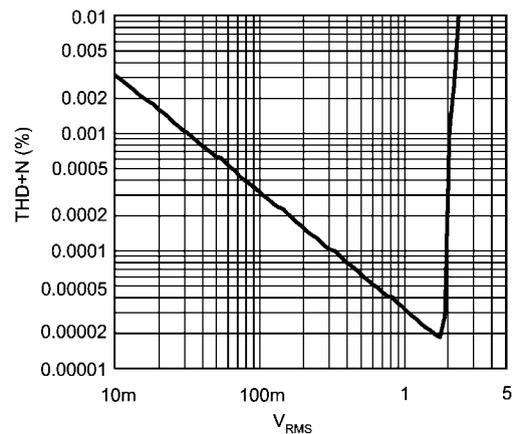**THD+N vs Output Voltage**
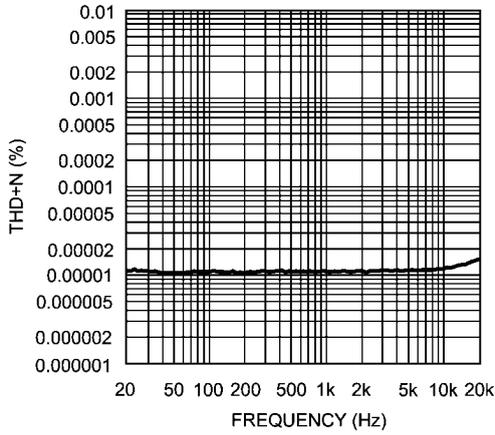$V_{CC} = -V_{EE} = 15V$, $R_L = 600\Omega$

THD+N vs Output Voltage
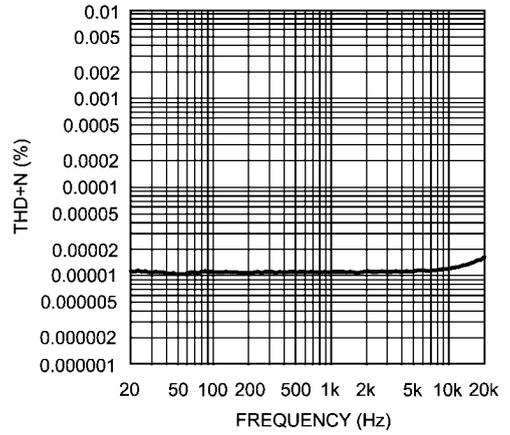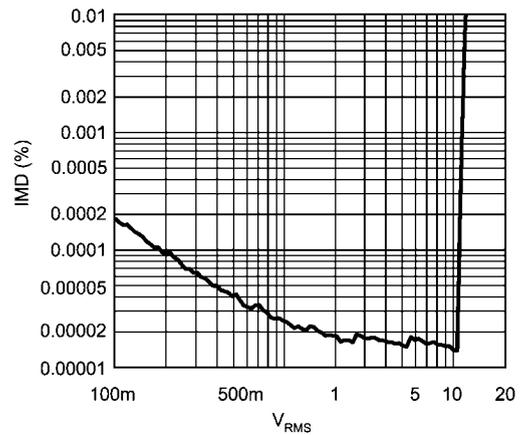$V_{CC} = -V_{EE} = 18V$, $R_L = 600\Omega$

THD+N vs Output Voltage
$V_{CC} = -V_{EE} = 5V$, $R_L = 600\Omega$

THD+N vs Frequency
$V_{CC} = -V_{EE} = 15V$,
$R_L = 2k\Omega$, $V_{OUT} = 3V_{RMS}$

300597d6

THD+N vs Frequency
$V_{CC} = -V_{EE} = 18V$,
$R_L = 2k\Omega$, $V_{OUT} = 3V_{RMS}$

300597d8

THD+N vs Frequency
$V_{CC} = -V_{EE} = 15V$,
$R_L = 600\Omega$, $V_{OUT} = 3V_{RMS}$
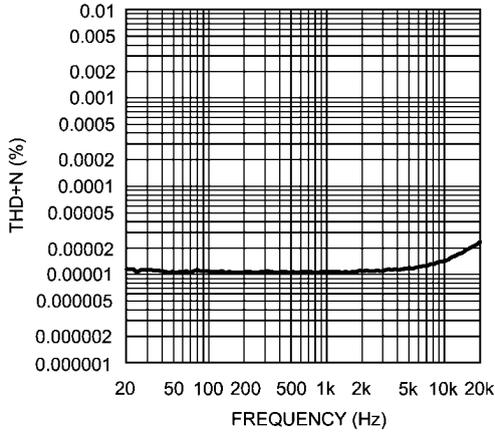
300597d7

THD+N vs Frequency
$V_{CC} = -V_{EE} = 18V$,
$R_L = 600\Omega$, $V_{OUT} = 3V_{RMS}$
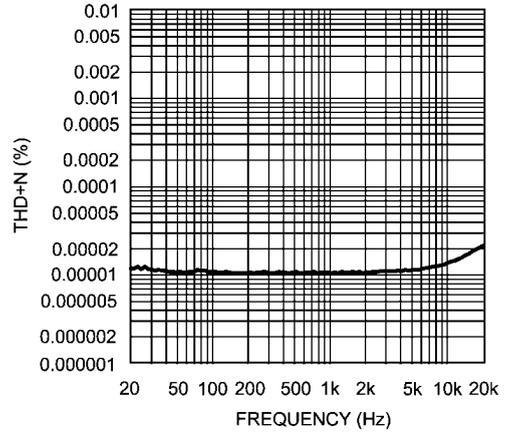
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IMD vs Output Voltage
$V_{CC} = -V_{EE} = 15V$, $R_L = 2k\Omega$
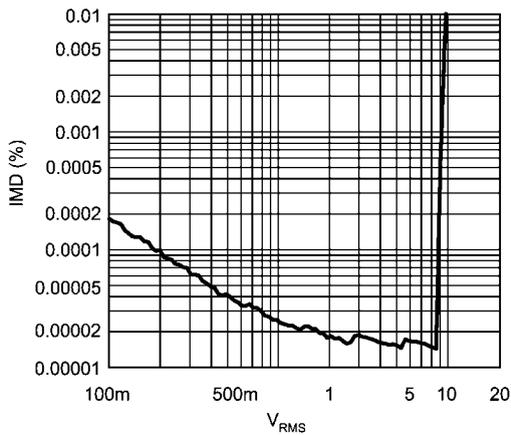
300597d1

IMD vs Output Voltage
$V_{CC} = -V_{EE} = 18V$, $R_L = 2k\Omega$

300597d3

IMD vs Output Voltage
$V_{CC} = -V_{EE} = 5V$, $R_L = 2k\Omega$

300597c9

IMD vs Output Voltage
$V_{CC} = -V_{EE} = 15V$, $R_L = 600\Omega$

300597d2

IMD vs Output Voltage
$V_{CC} = -V_{EE} = 18V$, $R_L = 600\Omega$

300597d4

IMD vs Output Voltage
$V_{CC} = -V_{EE} = 5V$, $R_L = 600\Omega$

300597d0

Voltage Noise Density vs Frequency

$V_S = 30V$
$V_{CM} = 15V$

0.88 nV/√Hz

300597e6

Current Noise Density vs Frequency

$V_S = 30V$
$V_{CM} = 15V$

2.8 pA/√Hz
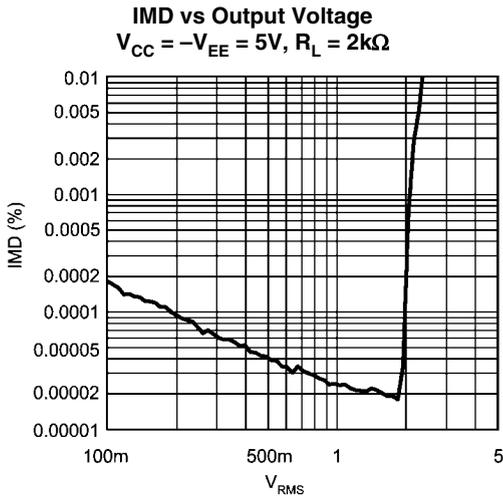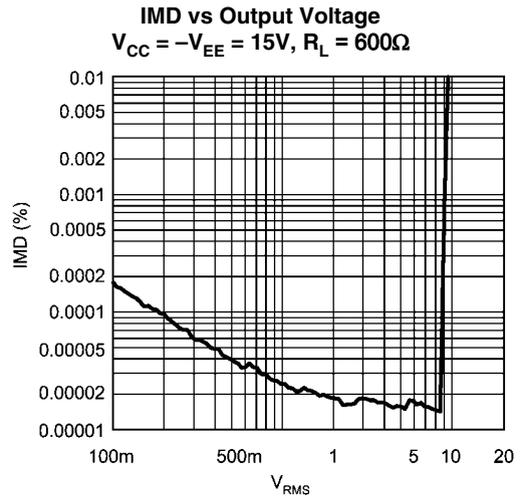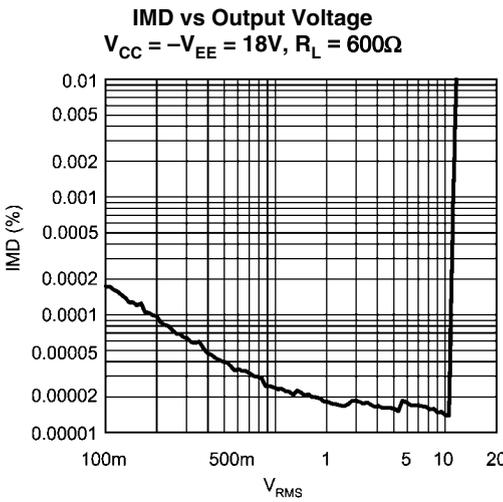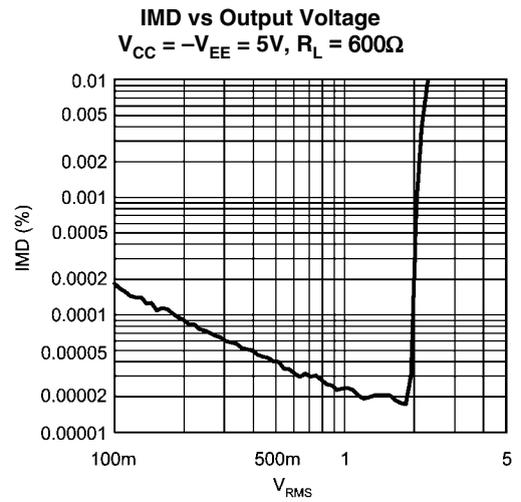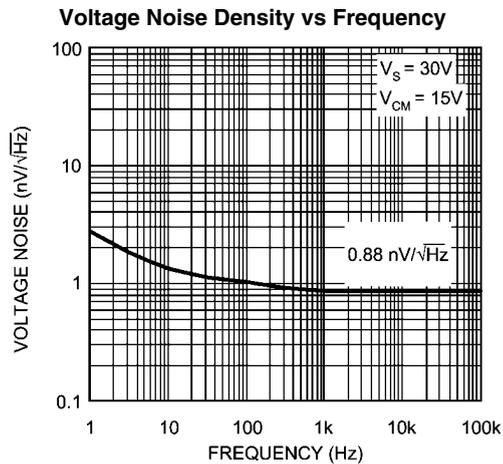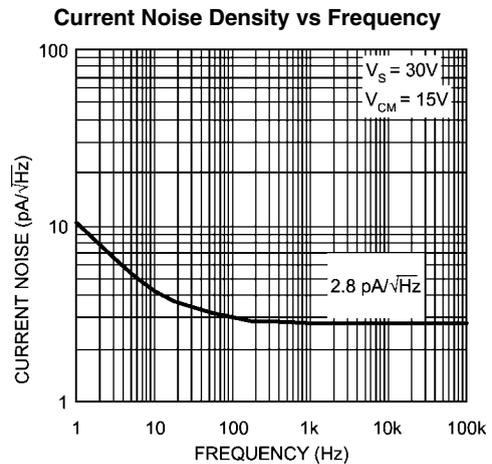
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PSRR vs Frequency
V$_{CC}$ = −V$_{EE}$ = 15V,
R$_L$ = 2kΩ, V$_{RIPPLE}$ = 200mVpp
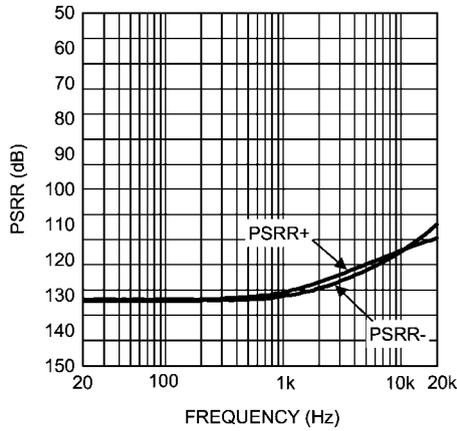
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+PSRR vs Frequency
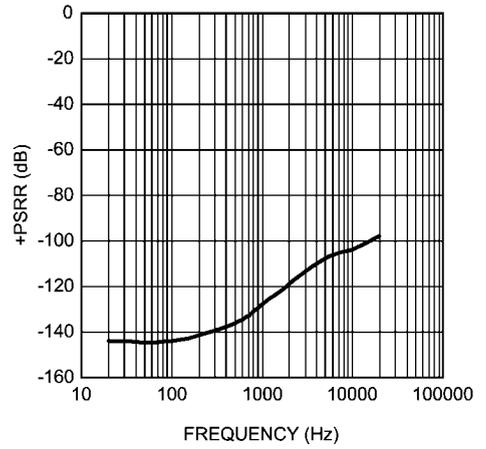
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—PSRR vs Frequency
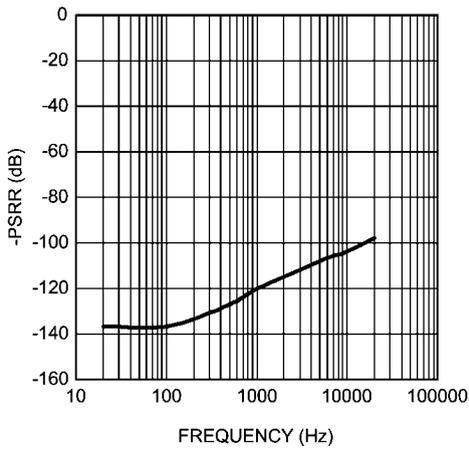
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Output Voltage vs Supply Voltage
R$_L$ = 2kΩ, THD+N = 1%
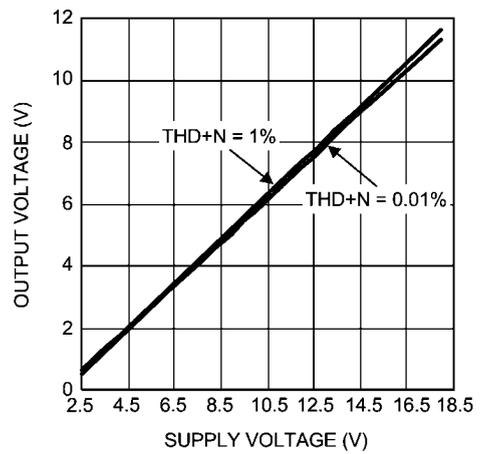
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Output Voltage vs Supply Voltage
R$_L$ = 600Ω, THD+N = 1%
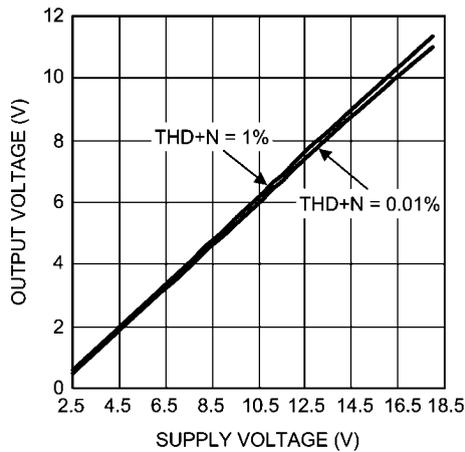
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Large-Signal Transient Response
A$_V$ = −1, C$_L$ = 100pF
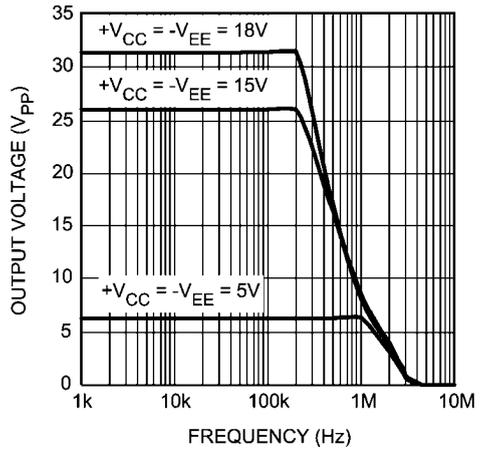
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Application Hints

OUTPUT DRIVE AND STABILITY

The LME49990 is unity gain stable from both input (both stable when gain = -1 or gain = 1). It able to drive resistive load 600Ω with output circuit with a typical 27mA. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straight forward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

The effective load impedance (including feedback resistance) should be kept above 600Ω for fast settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1kΩ to 2 kΩ range whenever practical.

OUTPUT COMPENSATION

In most of the audio applications, the device will be operated in a room temperature and compensation networks are not necessary. However, the consideration of output network as shown in Figure 3 may be taken into account for some of the high performance audio applications such as high speed data conversion or when operating in a relatively low junction temperature. The compensation network will also provide a small improvement in settling time for the response time demanding applications.
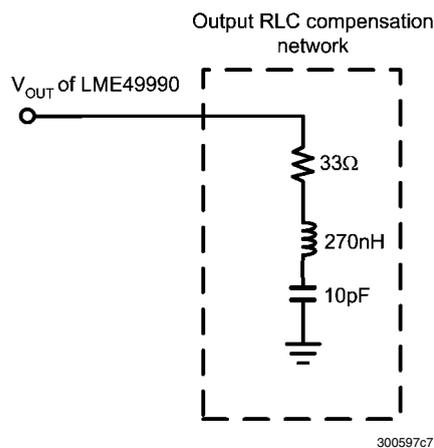
FIGURE 3. LME4990 Output Compensation Network

SUPPLY BYPASSING

To achieve a low noise and high-speed audio performance, power supply bypassing is extremely important. Applying multiple bypass capacitors is highly recommended. From experiment results, a 10µF tantalum, 2.2µF ceramic, and a 0.47µF ceramic work well. All bypass capacitors leads should be very short. The ground leads of capacitors should also be separated to reduce the inductance to ground. To obtain the best result, a large ground plane layout technique is recommended and it was applied in the LME49990 evaluation board.

Typical Applications

Balanced Input Mic Amp
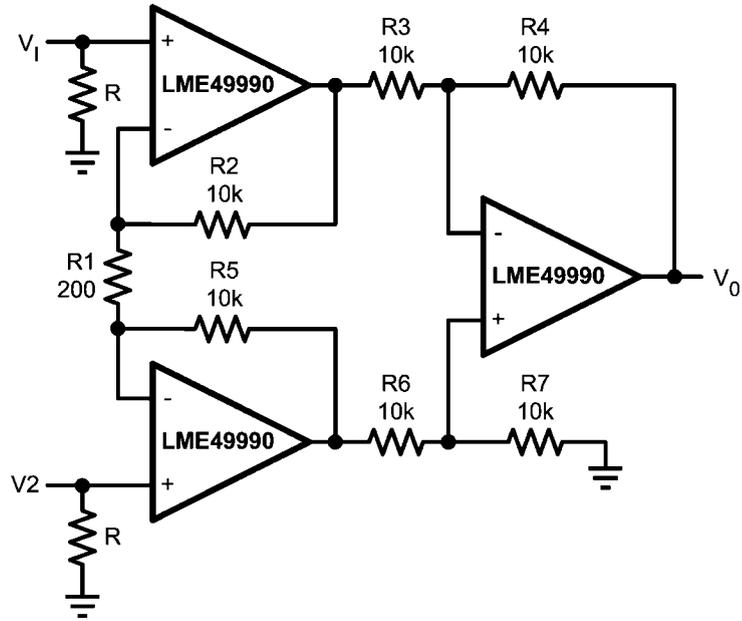
If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:

V0 = 101(V2 − V1)
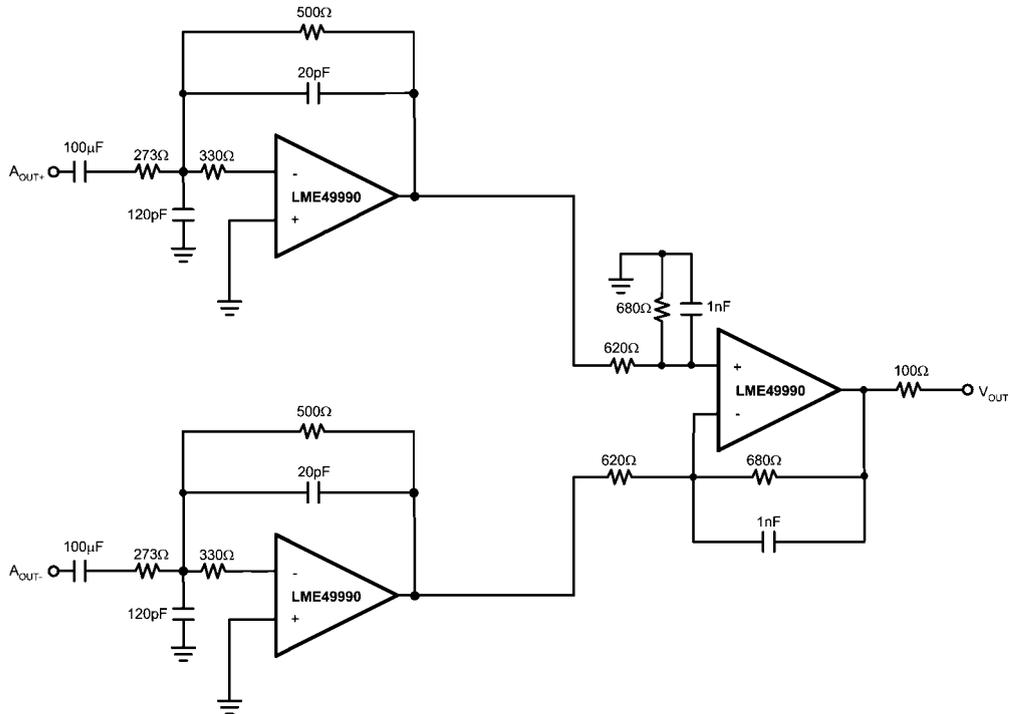
MFB 3rd Order PCM LPF

Application Information

SETTLING TIME AND SLEW RATE MEASUREMENTS

The settling time of LME49990 may be verified using the test circuit in Figure 4. The LME49990 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LME49990's output voltage is equal to the input voltage, the voltage on the PROBE 1 will be zero. Any voltage appearing at this point will represent an error. And the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy (See Settling Time – Output Swing photo). For a 10V input signal, settling time to 0.01% (1mV) will occur when the displayed error is less than 0.5mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LME49990's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well.

It is important to note that the oscilloscope input amplifier may be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. The signal generator used for this measurement must be able to drive 50Ω with a very clean $\pm10V_{PP}$ square wave.

The Slew Rate of LME49990 tells how fast it responses to a transient or a step input. It may be measured by the test circuit in Figure 5. The Slew Rate of LME49990 is specified in close-loop gain = -1 when the output driving a $1k\Omega$ load at $20V_{PP}$. The LME49990 behaves very stable in shape step response and have a minimal ringing in both small and large signal step response (See Typical Performance Characteristic). The slew rate typical value reach as high as $\pm18V/\mu S$ was measured when the output reach -20V refer to the start point when input voltage equals to zero.
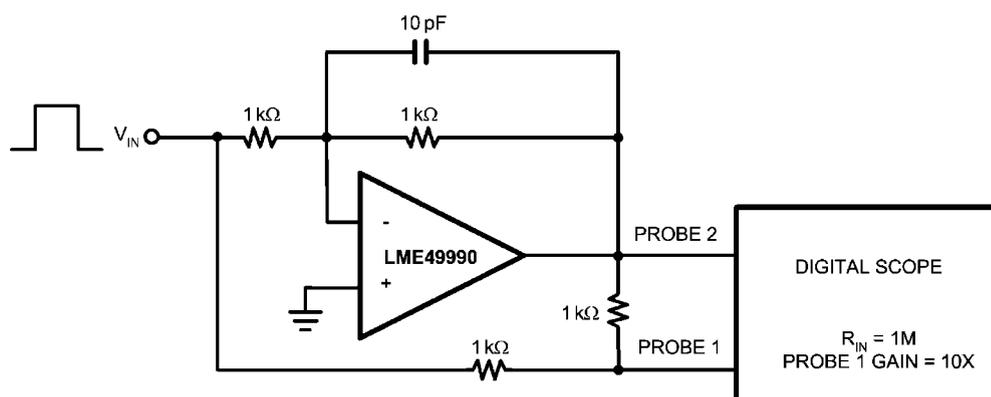
FIGURE 4: Settling Time Test Circuit
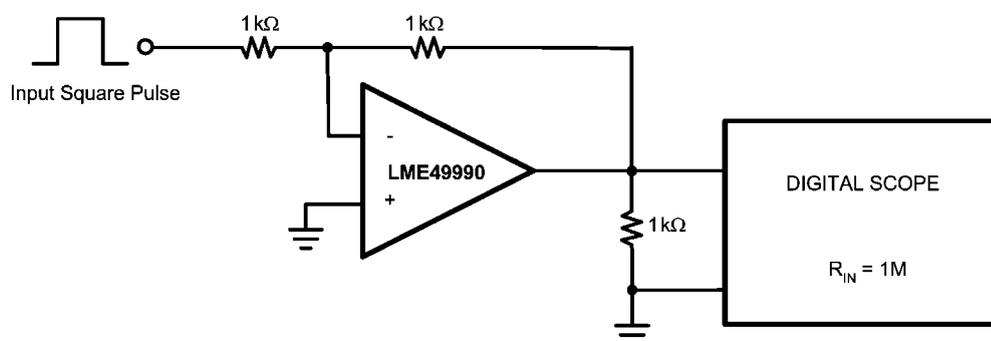
FIGURE 5: Slew Rate Test Circuit

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49990 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49990's low residual distortion is an input referred internal error. As shown in Figure 6, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 6.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

Distortion Signal Gain = 1+(R2/R1)

Actual Distortion = AP Value/100
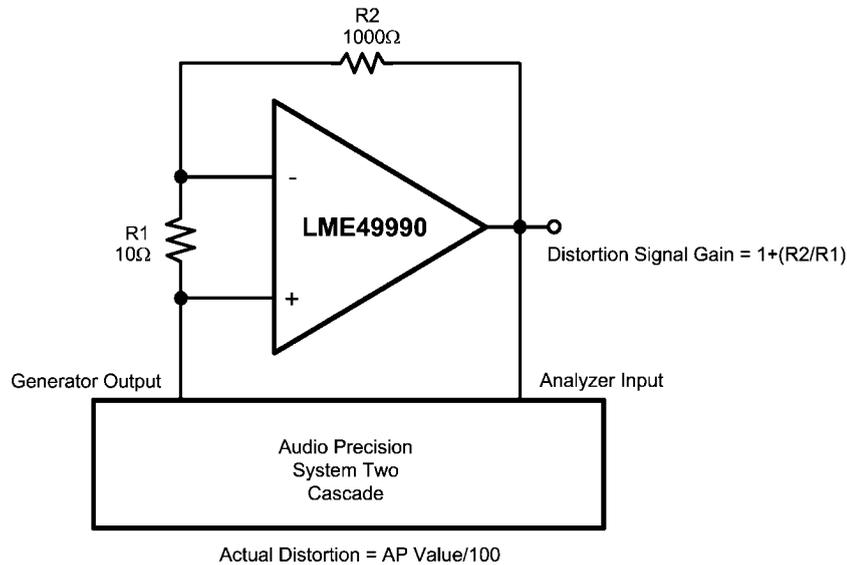
30059707

FIGURE 6: THD+N and IMD Distortion Test Circuit

Revision History

Rev	Date	Description
1.0	12/16/09	Initial released.
1.01	01/08/10	Input text edits.
1.02	02/08/11	Added the SDB08B package.
1.03	02/15/11	Updated the Ordering Information table.
1.04	07/08/11	Added the MA and LLP Top Markings and input text edits.
1.05	07/11/11	Added the θ_{JA} (LLP) limit = 52.5°C/W (under Thermal Resistance) in the Abs. Max. section
1.06	07/12/11	Added "The exposed pad (DAP) of unit should NOT be grounded. (It should be left floating)", in the Applications section (cover page).
1.07	07/21/11	Changed "The exposed pad (DAP) of unit should NOT be grounded. (It should be left floating)", in the Applications section (cover page). **Changed to:** "The exposed pad (DAP) of unit should not be grounded. It is internally connected to V_{EE}".

Physical Dimensions inches (millimeters) unless otherwise noted

4.9±0.1
[.193±.004]
NOT INCLUDING MOLD FLASH,
PROTRUSION OR GATE BURRS.
0.15[.006] MAX PER END

8X (0.6)
[.02]

8X (2.2)
[.09]

(5.2)
[.20]

6X (1.27)
[.05]

RECOMMENDED LAND PATTERN

6±0.2
[.236±.008]

3.9±0.1
[.154±.004]
NOT INCLUDING
MOLD FLASH,
PROTRUSION
OR GATE BURRS

PIN 1 ID

1.35-1.75
[.053-.069]
TYP

6X 1.27
[.050]

(1.45)
[.057]

0.1[.004] C

45° X 0.25-0.50
[.010-.020]

R0.18±0.02
[.007±.0008]

R0.23±0.02
[.009±.0008]

TIE BAR

0.25
[.010]
GAGE PLANE

0°-8°

8X 0.35-0.51
[.0138-.0200]

0.10-0.25
[.004-.010]
TYP

0.41-1.27
[.016-.050]

SEATING
PLANE

0.190-0.248
[.0075-.0098]
TYP

(1.04)
[.041]

0.25[.010]M C A⑤ B⑤

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

M08A (Rev M)

Dual-In-Line Package
Order Number LME49990MA
NS Package Number M08A

(1.68)

(4.8)

(2.34)

(8X 1.0)

(8X 0.3)

(6X 0.65)
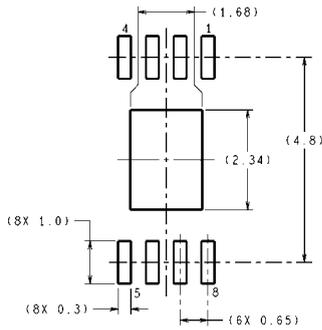
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN

PIN 1 INDEX AREA

5.4±0.1

3.4±0.1

TOP SIDE OF PACKAGE

(0.1)

0.8 MAX

(0.2)

1.68±0.1

PIN 1 ID

(45° X 0.25)

2.34±0.1

8X 0.8±0.1

8 X 0.3±0.05

6X 0.65

0.1M C A⑤ B⑤

2X 1.95
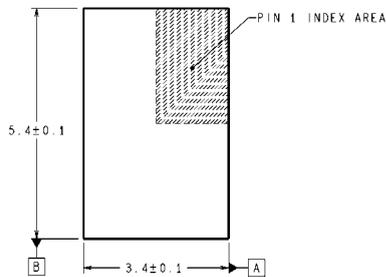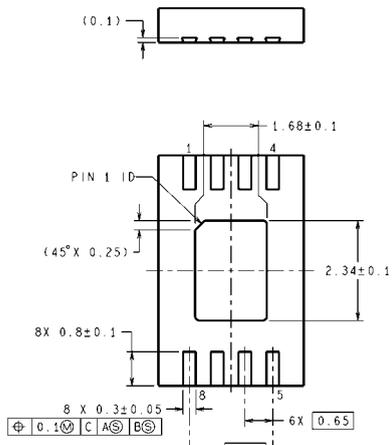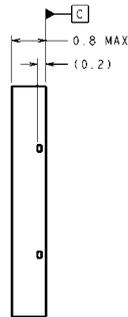
BOTTOM SIDE OF PACKAGE

SDB08B (Rev A)

Dual-In-Line Package
Order Number LME49990SD
NS Package Number SDB08B

Notes

Notes

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